REMARKS

Applicant wishes to thank the Examiner for allowance of claims 39-78. Claims 21 and 33 have been amended. Claims 1-76 remain in the application. No claims have been canceled. No claims have been added.

Claim Objections

Claim 33 was objected to having a typographical error. The word "be" has been amended to "been" as suggested. Applicant submits claim 33 is now in proper form.

35 U.S.C. §102 Rejections

Claims 1, 2, 4-7, 10-12, 14-22, 24-31 and 3-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Fairbanks U.S. Pat. No. 6,191,658 ("Fairbanks")

Fairbanks describes an oscillator circuit in CMOS using a 2:1 PMOS to NMOS width ratio. Specifically, the disclosed oscillator is implemented using circuit elements containing a keeper having two nodes and two pairs of inverters. The outputs of one pair of inverters are tied to a first node of the keeper and the outputs of the other pair are tied to a second node. A preferred embodiment shows that the oscillator circuit contains four such circuit elements arranged in a ring such that the outputs of each circuit element are coupled to two neighbor circuit elements, specifically, the output of a given circuit element is connected the inputs of its two neighboring circuit elements. Fairbanks' oscillator uses C-elements (250A, 250B, 250C or 250D in Figure 3b), each causing both the rising and falling transitions on any wire in the system.

Independent Claim 1

Independent claim 1 contains the limitation "...the cell on one end generates the rising edge and the cell on the other end generates the falling edge." (Emphasis added). Applicant's claim 1 has the rising transition of a clock wire achieved by one cell on one end of the wire and the falling transition of the same clock wire achieved by another cell on another end of the clock wire. By way of example and not by way of limitation, see at least in Figure 4 and paragraph 57 of the specification. On the contrary, each wire in Fairbanks has only one element, the C-element logic gate which causes both the rising and falling transition. As an example, this is illustrated in Figure 3b (Fairbanks) where the rising and falling transitions in the line connecting inputs 301A, 302C and output 306D are controlled by the C-element 250D. As such, applicant submits that claim 1 is

not anticipated by Fairbanks and respectfully requests the withdrawal of the claim rejection.

Independent claim 11

Independent claim 11 contains the limitation "...each of said plurality of cells is coupled to multiple adjacent complementary ones of said plurality of cells by different clock wires ..." (Emphasis added). Fairbanks, as explained, describes an oscillator consisting of C-element logic gates interconnected to each other. Specifically, the rising and falling transitions in each interconnecting wire are controlled by the output of the C-element or logic gate to which the wire is attached. Thus, as illustrated in Figure 3b (Fairbanks), the oscillator consists of four identical C-elements. On the contrary, Applicant claims "each of said plurality of cells is coupled to multiple adjacent complementary ones of said plurality of cells", thus indicating that the adjacent cells connected to any one cell is complementary to and not the same as that cell. By way of example and not by limitation, see at least in Figure 4 of the specification which shows pull-up cells connected to pull-down cells. As such, applicant submits that claim 11 is not anticipated by Fairbanks and respectfully requests the withdrawal of the claim rejection.

Independent claim 21

Independent claim 21 contains the limitation "... wherein each of the plurality of cells oscillate dependent upon clock signals received from multiple of others of the plurality of cells; and a plurality of sets of synchronous logic, distributed over said integrated circuit, coupled to be clocked by said clock generator." (emphasis added). Fairbanks teaches in Figures 3A and 3B that each element is configured such that a logic signal traversing a path that begins and ends at the same output is logically inverted an odd number of times. In Fairbanks, the signals need not be the same phase and frequency

traveling along the wires and are not true clock signals as in Applicant's claim 21. In Fairbanks each cell does not truly oscillate "depend upon clock signals received from others" because they are logic signals and each neighboring cell's inputs and output are connected to each others' output and inputs respectively. There is a logical dependency but no clock signal dependency as claimed. For example, in Figure 3B (Fairbanks), output of cell 250A becomes input of 250B which outputs at 306B and inputs back into 302A. By way of example but not by limitation, see at least in Figures 4 and 7 where one clock signal wire connects between two neighboring cells. Applicant's claimed invention is truly a "synchronous" logic "distributed" over the integrated circuit "coupled" to be clocked by the clock generator. As such, applicant submits that claim 21 is not anticipated by Fairbanks and respectfully requests the withdrawal of the claim rejections.

Independent claim 30

Independent claim 30 contains the limitation "... a plurality of cells that, responsive to an averaging of a previous clock edge produced by said plurality of cells, detect when to produce the next clock edge, ... a plurality of sets state holding elements each having a clock input, each clock input of each of said sets coupled to a different one of said plurality of clock wires." (Emphasis added). The elements disclosed in Fairbanks are configured such that a logic signal traversing a path that begins and ends at the same output is logically inverted an odd number of times. Fairbanks uses cells that produce an output value only once both inputs reach a logical (digital) state. Fairbanks does not teach that the cells are "responsive" to "averaging of previous clock edge" and "detect when to produce the next clock edge". As described in Fairbanks, a logic signal starting at an output traverses a closed path and inverted three times and returns to the original point (Fairbanks, Col. 4, lines 40-48). Further, the logic signal is set in a predetermined path and time course and the oscillator frequency is only increased by reducing the load

driven by the transistors through reducing the capacitance found in the drain diffusion regions shared by two transistors (Fairbanks, Col. 4, lines 59-68). Thus, Fairbanks does not "respond" to "averaging" of previous clock edges to decide when to produce the next clock edge. Cells in claim 30 collectively average previous clock edge produced by a plurality of cells and detect when to produce the next clock edge. Fairbanks merely shows logic dependencies of logic signals and logic inputs. As such, Applicant submits that claim 30 is not anticipated by Fairbanks and respectfully requests withdrawal of the claim rejection.

Dependent claims 2, 4, 7, 10, 12, 14-20, 22, 24-29, 31, and 33-38

Dependent claims 2, 4, 7, 10, 12, 14-20, 22, 24-29, 31, and 33-38 each depend from one of the independent claims described above. For at least this reason, each dependent claim incorporates a limitation present in the corresponding independent claim which is not anticipated by Fairbanks. For at least this reason, applicant respectfully requests the withdrawal of the rejection of the dependent claims.

35 U.S.C. 103(a) Rejections

Claims 3, 13, 23, and 32 are rejected under 35 U.S.C. 103(a) as being unpatenable over Fairbanks in view of Graef U.S. Pat. No. 6,305,001 ("Graef")

Dependent claims 3, 13, 23, 32

Dependent claims 3, 13, 23 and 32 depend from independent claims 1, 11, 21, and 30 respectively and thus contain the limitations therein. Graef describes a method for planning the clock distribution network in the conceptual design phase of an ASIC device. Graef fails to teach or suggest that in a clock wire, one element on one end is responsible for causing the rising transition edge while another element on another end is responsible for causing the falling transition edge, where the elements on the two ends of the wire are complementary and not the same. Since Graef fails to cure the deficiency in Fairbanks, the combination of Graef and Fairbanks will not teach the limitation as disclosed in the independent claims as discussed above. As such, Applicant submits that the dependent claims are valid and respectfully requests the withdrawal of the rejections of the claims.

Allowable Subject Matter

While Applicant thanks the Examiner for allowing Claims 39-78 Applicant wants to clarify the record with regard to the statements in the Office Action concerning the claims 39, 75, 52 and 62. The Office Action could be misconstrued to suggest that claims 39 and 75 are limited to the configuration of a distributed clock generator as shown in Figure 6-7, "having specific structural limitations such as ... each of the plurality of clock wires coupling one of the plurality of terminals of one of the plurality of cells to one of the plurality of terminals of another of the plurality of cells" (Office Action 11/02/05, p. 5). Similarly, the Office Action could be misconstrued to suggest that claims 52 is limited to the configuration of a distributed clock generator as shown in Figure 6-7,

"having specific structural limitations such as ... and being configured in combination with the rest of the limitations of the base claim and any intervening claims" (Office Action 11/02/05, p. 5). Further, the Office Action could be misconstrued to suggest that claims 62 is limited to the configuration of a distributed clock generator as shown in Figure 6-7, "having specific structural limitations such as ... to cause another clock edge transition of the clock signals to substantially simultaneously occur some delay time after each of the single clock edge transition times." (Office Action 11/02/05, p. 6-7).

Applicant would like to clarify that the Office Action merely uses the elements in the figures as examples and that these examples are not intended and should not be used to read limitations into the claims.

As iterated in the response to the prior Office Action dated 01/13/05 and Office Action dated 6/14/05, Applicant submits that according to MPEP §2111.01, claims must be given their "broadest reasonable interpretation" while examined by the USPTO and that "the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification"; also "ordinary, simple English words whose meaning is clear and unquestionable, absent any indication that their use in a particular context changes their meaning, are construed to mean exactly what they say"; and "a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." The only exception is "when an element is claimed using language falling under the scope of 35 U.S.C. 112, 6th paragraph." However, none of the claims are means plus function claims which would prompt any reference to the specification to clarify the scope of what is claimed.

For at least these reasons, Applicant feels it necessary to clarify the meaning of the statements in the Office Action and request the Examiner to indicate if the meaning is contrary to what is stated above.

CONCLUSION

Applicant respectfully submits that the rejections have been overcome by the remarks, and that the Claims are in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the Claims be allowed.

Invitation for a telephone interview

The Examiner is invited to call the undersigned at 408-720-8300 if there remains any issue with allowance of this case.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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